



# PEMD2

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 22 k $\Omega$ , R2 = 22 k $\Omega$

13 March 2023

Product data sheet

## 1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PEMH1

PNP/PNP complement: PEMB1

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

## 3. Applications

- Low current peripheral driver
- Controlling IC inputs
- Replaces general-purpose transistors in digital applications

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
V <sub>CEO</sub>	collector-emitter voltage	open base	[1]	-	-	50	V
I <sub>O</sub>	output current		[1]	-	-	100	mA
R1	bias resistor 1 (input)		[2]	15.4	22	28.6	k $\Omega$
R2/R1	bias resistor ratio		[2]	0.8	1	1.2	

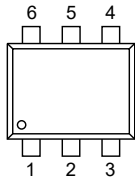
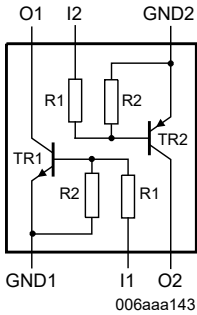
[1] For the PNP transistor with negative polarity.

[2] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 22 k $\Omega$ , R2 = 22 k $\Omega$ 

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p style="text-align: center;"><b>SOT666</b></p>	 <p style="text-align: center;">006aaa143</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">PEMD2</a>	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	<a href="#">SOT666</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PEMD2	D4

## 8. Limiting values

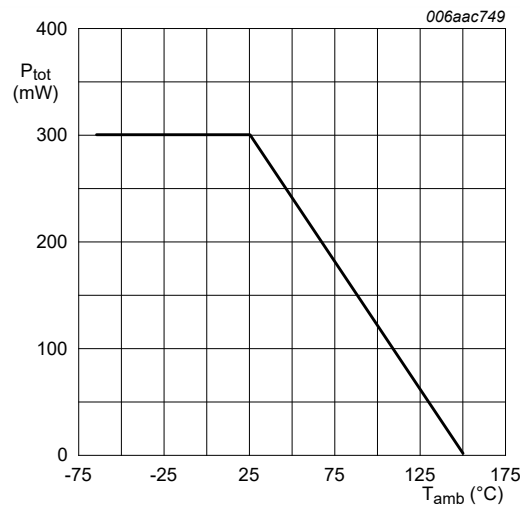
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
$V_{CBO}$	collector-base voltage	open emitter	[1]	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	[1]	-	50	V
$V_{EBO}$	emitter-base voltage	open collector	[1]	-	10	V
$V_i$	input voltage	TR1 (NPN)		-10	40	V
		TR2 (PNP)		-40	10	V
$I_O$	output current		[1]	-	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[2]	-	200	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[2]	-	300	mW
$T_j$	junction temperature			-	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C

[1] For the PNP transistor with negative polarity.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

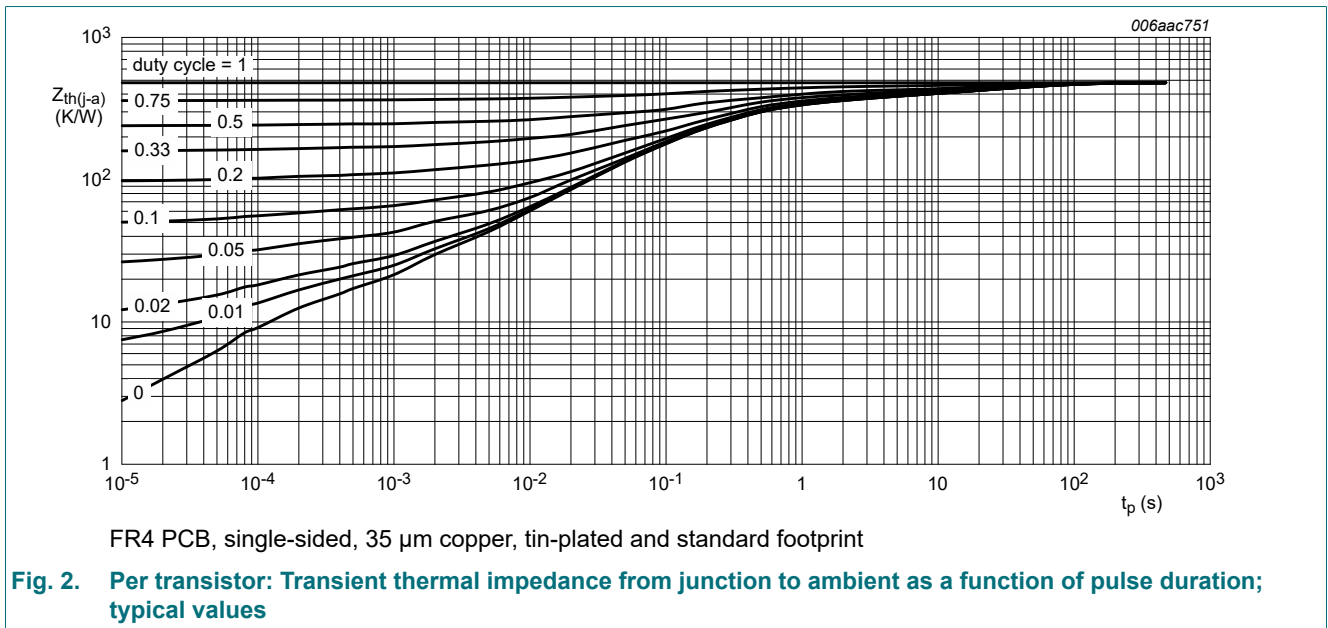
**Fig. 1. Per device: Power derating curve**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.



## 10. Characteristics

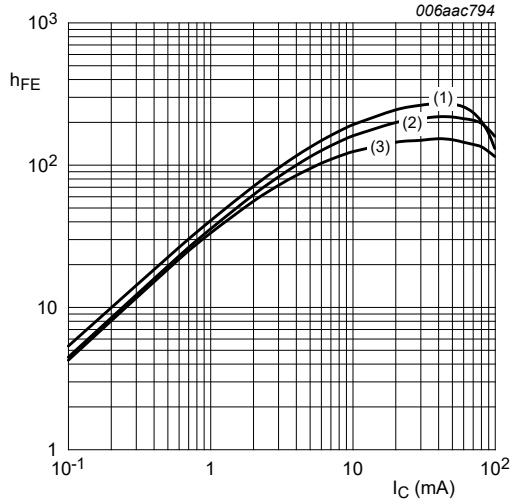
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu\text{A}$ ; $I_E = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}$ ; $I_B = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	50	-	-	V
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	-	100	nA
		$V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	[1]	-	-	5	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$ ; $I_C = 0 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	-	180	$\mu\text{A}$
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}$ ; $I_C = 5 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	60	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10 \text{ mA}$ ; $I_B = 0.5 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}$ ; $I_C = 100 \mu\text{A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}$ ; $I_C = 5 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$		2.5	1.7	-	V
R1	bias resistor 1 (input)		[2]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[2]	0.8	1	1.2	
<b>TR1 (NPN)</b>							
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ; $f = 1 \text{ MHz}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$		-	-	2.5	pF
$f_T$	transition frequency	$V_{CE} = 5 \text{ V}$ ; $I_C = 10 \text{ mA}$ ; $f = 100 \text{ MHz}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[3]	-	230	-	MHz
<b>TR2 (PNP)</b>							
$C_c$	collector capacitance	$V_{CB} = -10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ; $f = 1 \text{ MHz}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$		-	-	3	pF
$f_T$	transition frequency	$V_{CE} = -5 \text{ V}$ ; $I_C = -10 \text{ mA}$ ; $f = 100 \text{ MHz}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[3]	-	180	-	MHz

[1] For the PNP transistor with negative polarity.

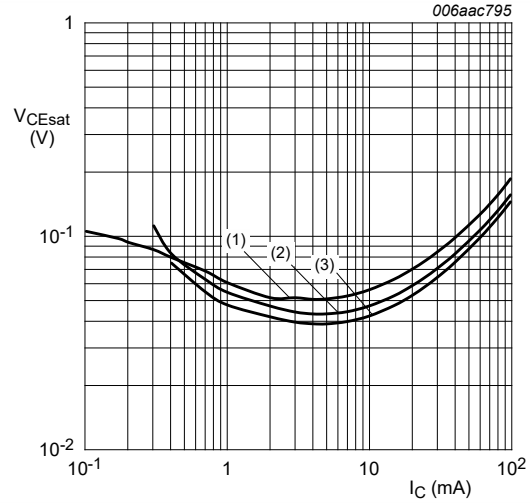
[2] See section "Test information" for resistor calculation and test conditions.

[3] Characteristics of built-in transistor



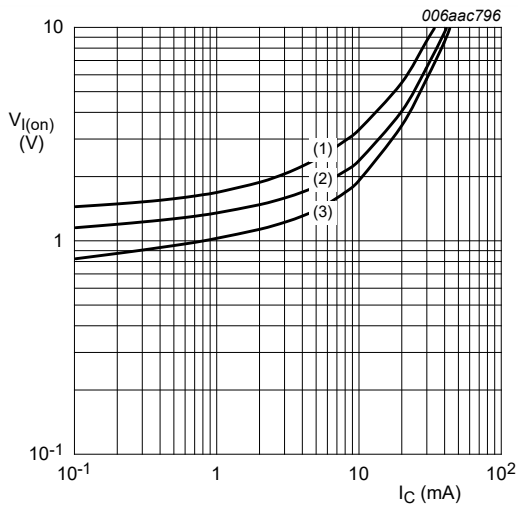
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values**



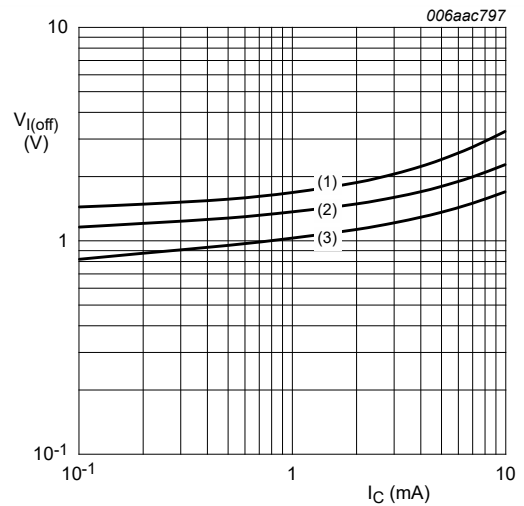
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



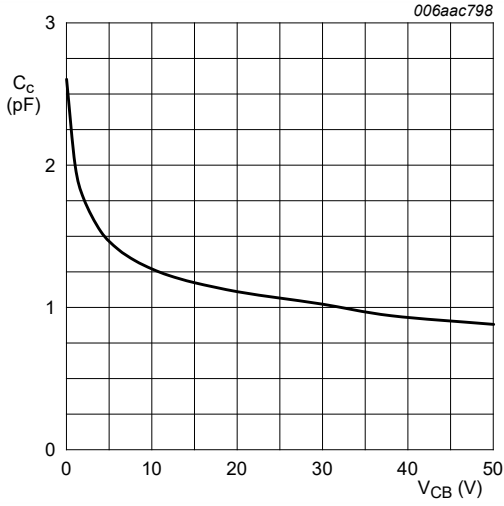
$V_{CE} = 0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values**



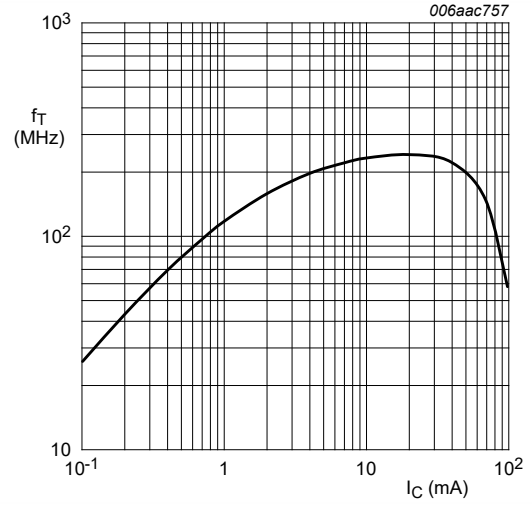
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



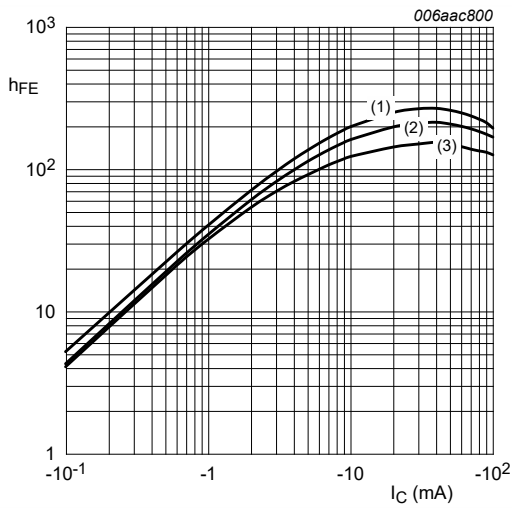
$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 7. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



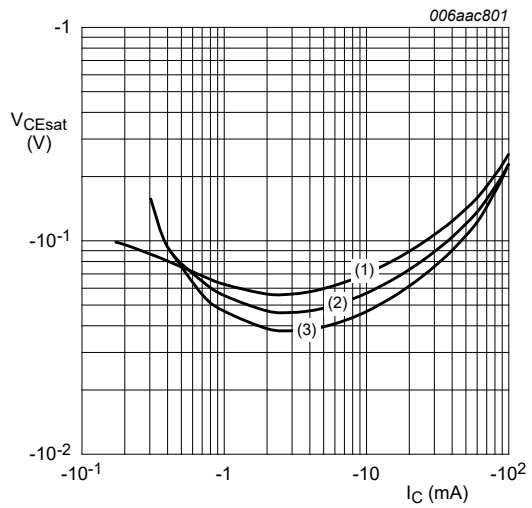
$f = 100 \text{ MHz}$   
 $T_{amb} = 25 \text{ }^\circ\text{C}$   
 $V_{CE} = 5 \text{ V}$

Fig. 8. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



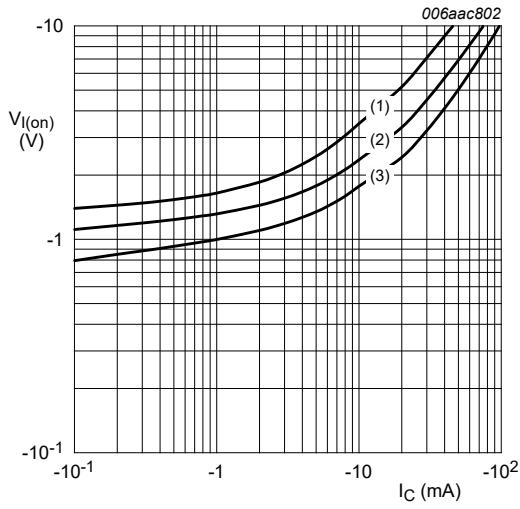
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig. 9. TR2 (PNP): DC current gain as a function of collector current; typical values



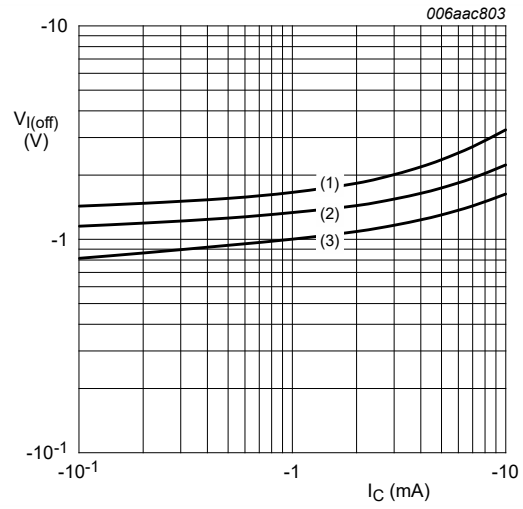
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig. 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



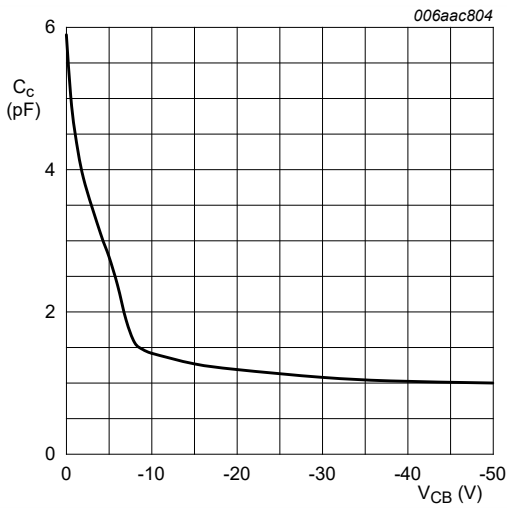
$V_{CE} = -0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ °C}$   
 (2)  $T_{amb} = 25 \text{ °C}$   
 (3)  $T_{amb} = 100 \text{ °C}$

**Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values**



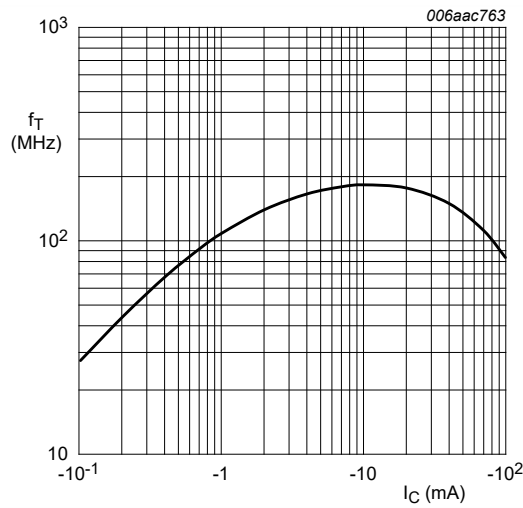
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ °C}$   
 (2)  $T_{amb} = 25 \text{ °C}$   
 (3)  $T_{amb} = 100 \text{ °C}$

**Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ °C}$

**Fig. 13. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values**



$f = 100 \text{ MHz}$   
 $T_{amb} = 25 \text{ °C}$   
 $V_{CE} = -5 \text{ V}$

**Fig. 14. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor**



## 11. Test information

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_3)}{R_1 \cdot I_3} - 1$$

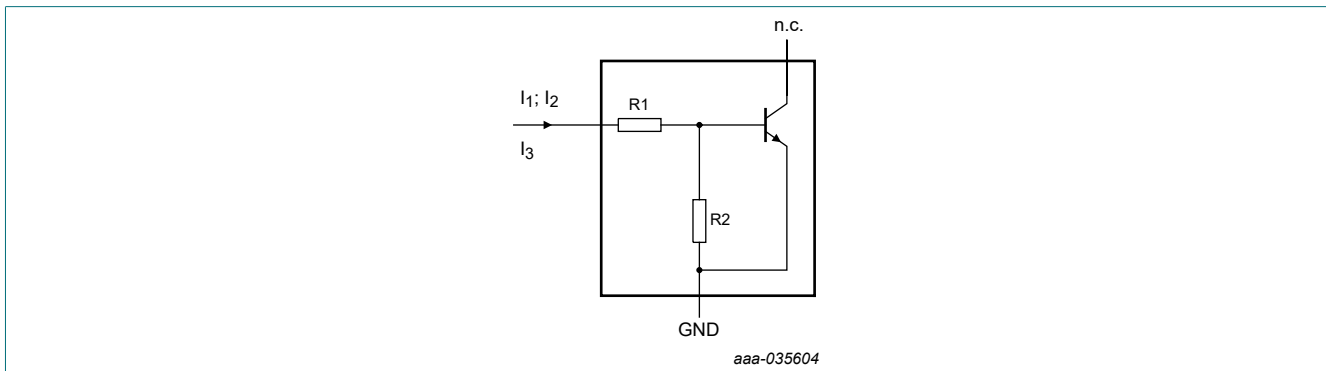


Fig. 15. TR1 (NPN): Resistor test circuit

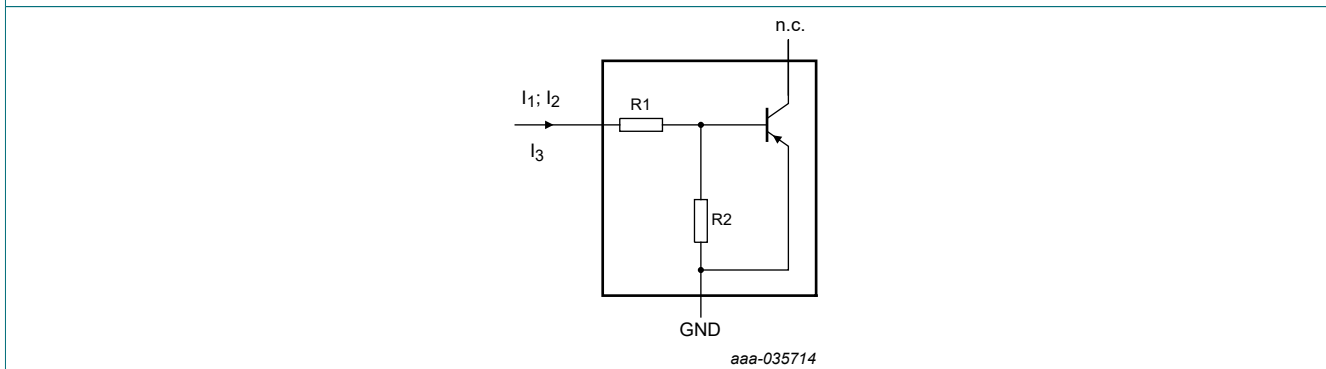


Fig. 16. TR2 (PNP): Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

PEMD2	R1 (kΩ)	R2 (kΩ)	Test conditions		
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>
TR1 (NPN)	22	22	160 μA	210 μA	-182 μA
TR2 (PNP)	22	22	-160 μA	-210 μA	182 μA

## 12. Package outline

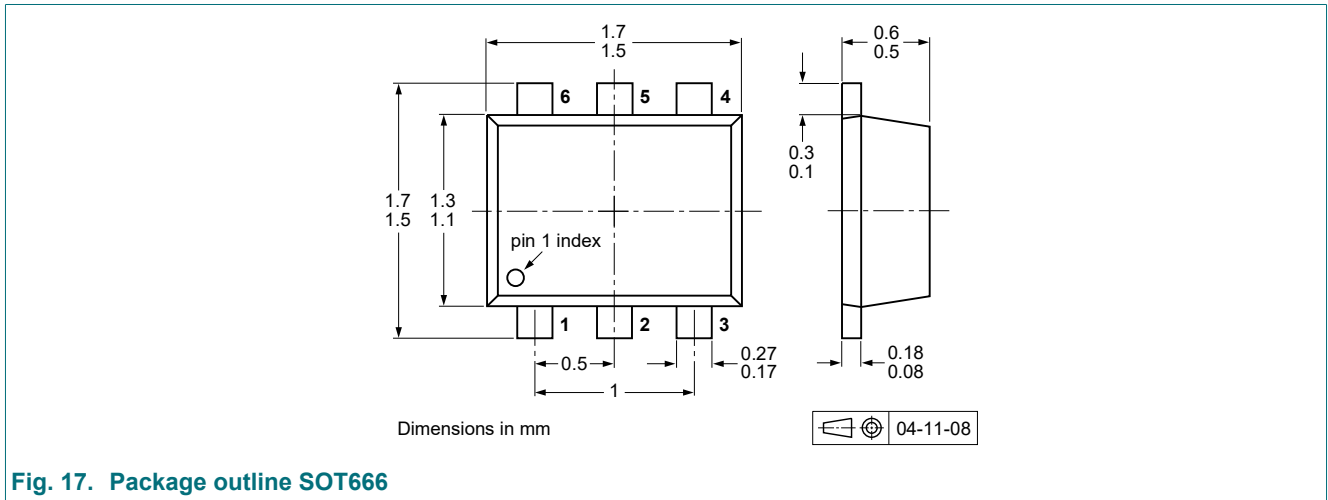


Fig. 17. Package outline SOT666

## 13. Soldering

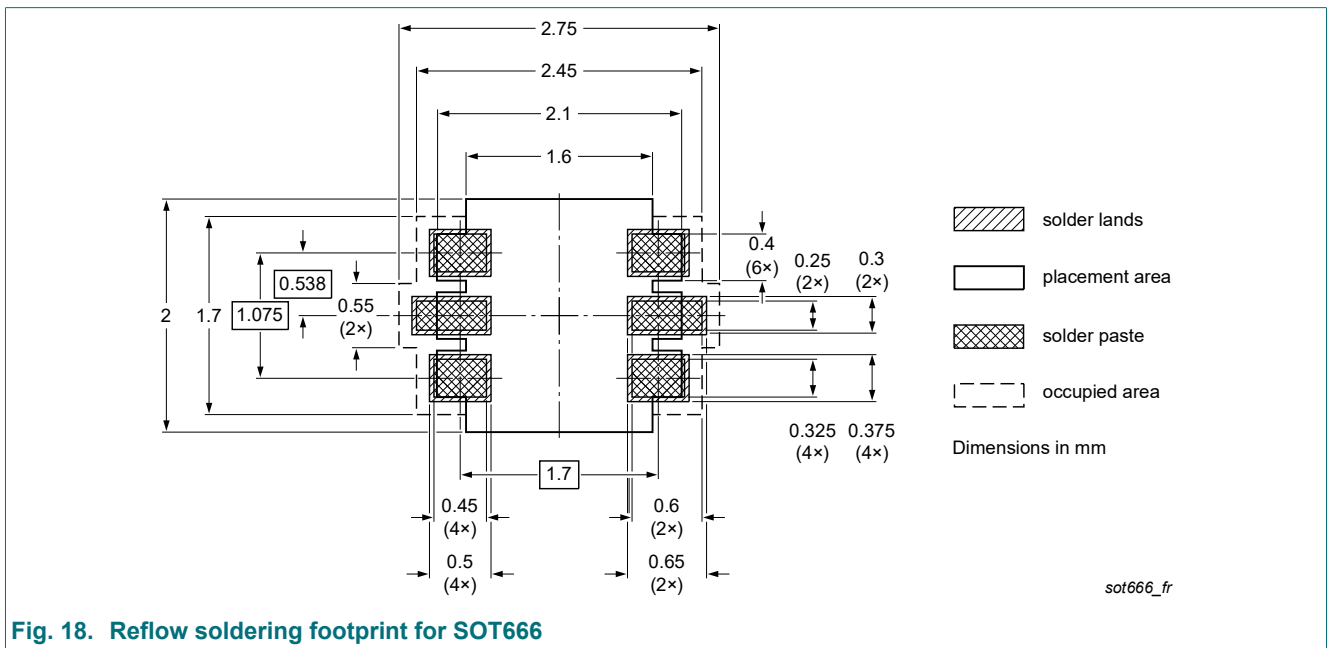


Fig. 18. Reflow soldering footprint for SOT666

## 14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PEMD2 v.9	20230313	Product data sheet	-	PEMD2_PIMD2_PUMD2 v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Product changed to non-automotive qualification.</li> <li>Family data sheet splitted to single type data sheets.</li> </ul>			
PEMD2_PIMD2_PUMD2 v.8	20131114	Product data sheet	-	PEMD2_PIMD2_PUMD2 v.7
PEMD2_PIMD2_PUMD2 v.7	20080924	Product data sheet	-	PEMD2_PIMD2_PUMD2 v.6
PEMD2_PIMD2_PUMD2 v.6	20042104	Product specification	-	PEMD2_PIMD2_PUMD2 v.5
PEMD2_PIMD2_PUMD2 v.5	20030606	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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